NCP6151/NCP6151A

Preliminary Datasheet

Dual Output 4 Phase +1/0 Phase Controller with single SVID Interface for Desktop and Notebook CPU Applications

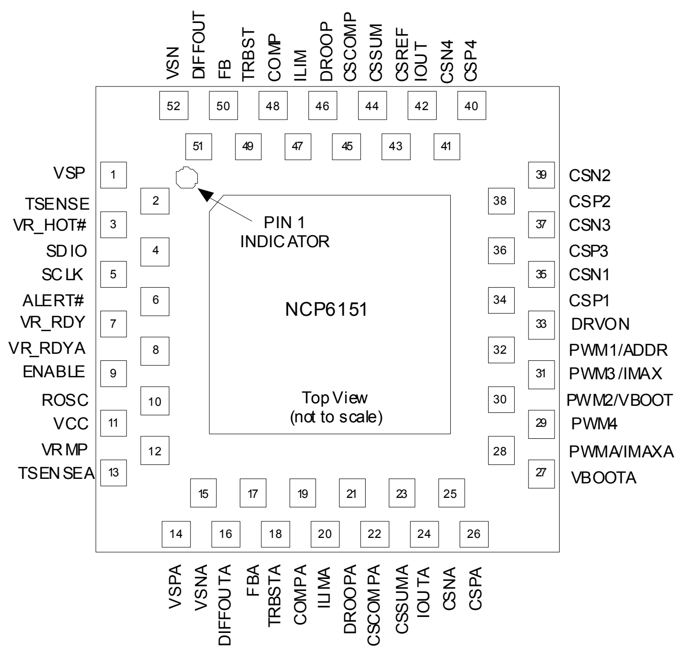
The NCP6151/NCP6151A dual output four plus one phase buck solution is optimized for Intel VR12 compatible CPUs. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed-forward, and adaptive voltage positioning to provide accurately regulated power for both Desktop and Notebook applications. The control system is based on Dual-Edge pulse-width modulation (PWM) combined with DCR current sensing providing the fastest initial response to dynamic load events and reduced system cost. It also sheds to single phase during light load operation and can auto frequency scale in light load while maintaining excellent transient performance.

Dual high performance operational error amplifiers are provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed-loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate current monitoring for droop and digital current monitoring.

NCP6151A support coupled inductor operation. It operates with 2 phases versus NCP6151 operating with single phase during PS1 mode.

Features

- Meets Intel VR12/IMVP7 Specifications
- Current Mode Dual Edge Modulation for Fastest Initial Response to Transient Loading
- Dual High Performance Operational Error Amplifier
- One Digital Soft Start Ramp for Both Rails
- Dynamic Reference Injection® (Patent #US07057381)
- Accurate Total Summing Current Amplifier(Patent #US006683441)
- DAC with Droop Feed-forward Injection(Patent Pending)
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase-to-Phase Dynamic Current Balancing
- “Lossless” DCR Current Sensing for Current Balancing
- Summed Thermally Compensated Inductor Current Sensing for Droop
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 100KHz – 1.0MHz



- Startup into Pre-Charged Loads While Avoiding False OVP

(QFN52 Dual Row Pin Package Shown)

Device	Package	Shipping
NCP6151D52MNR2G	QFN52 Dual Row	2500/Tape & Reel
NCP6151AD52MNR2G	QFN52 Dual Row	2500/Tape & Reel

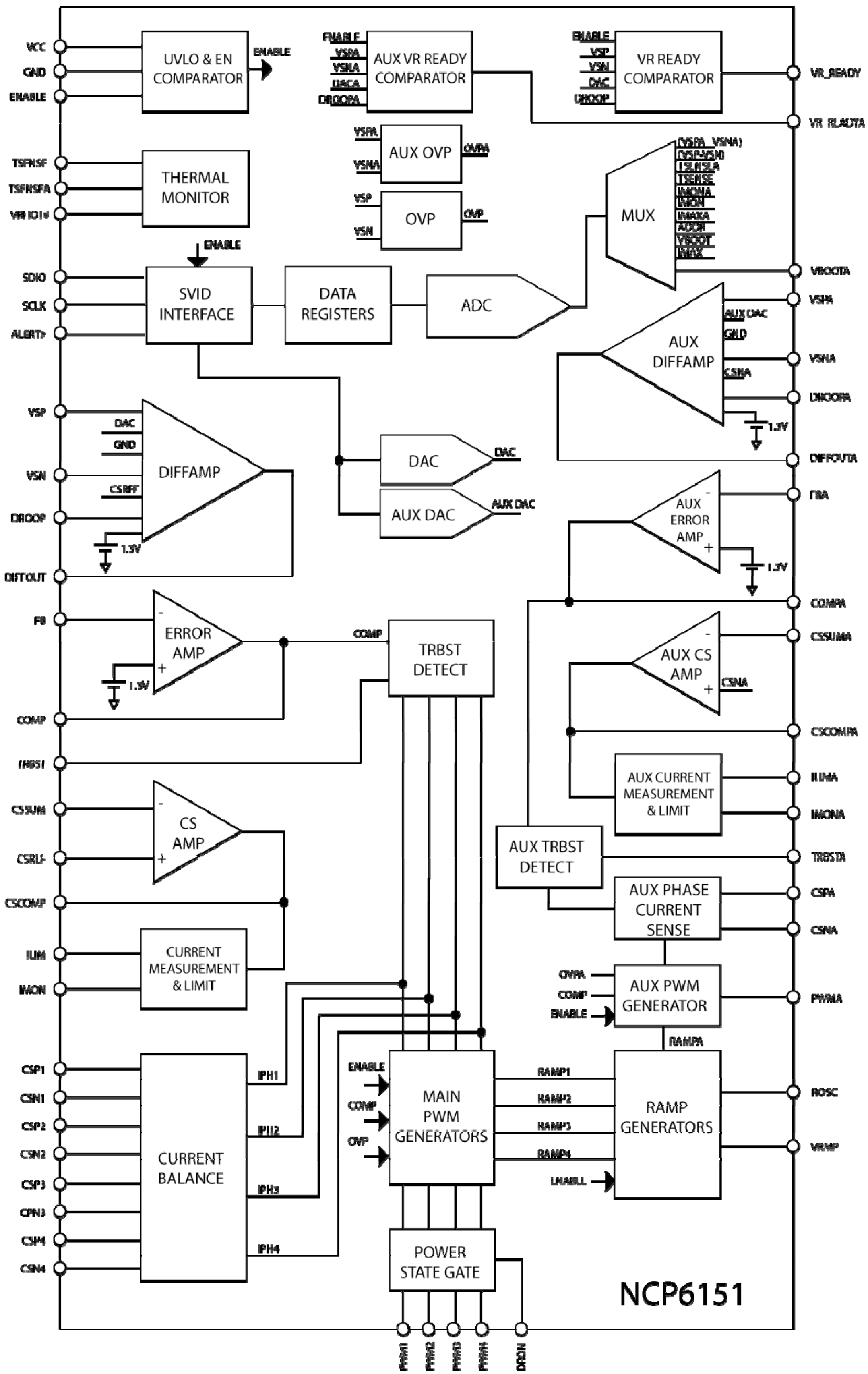
* Pb-free and Halide-free packages are available

- Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Pin Programming for Internal SVID parameters
- Over Voltage Protection (OVP) & Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- Dual Power Good Output with Internal Delays
- NCP6151A support coupled inductor operation

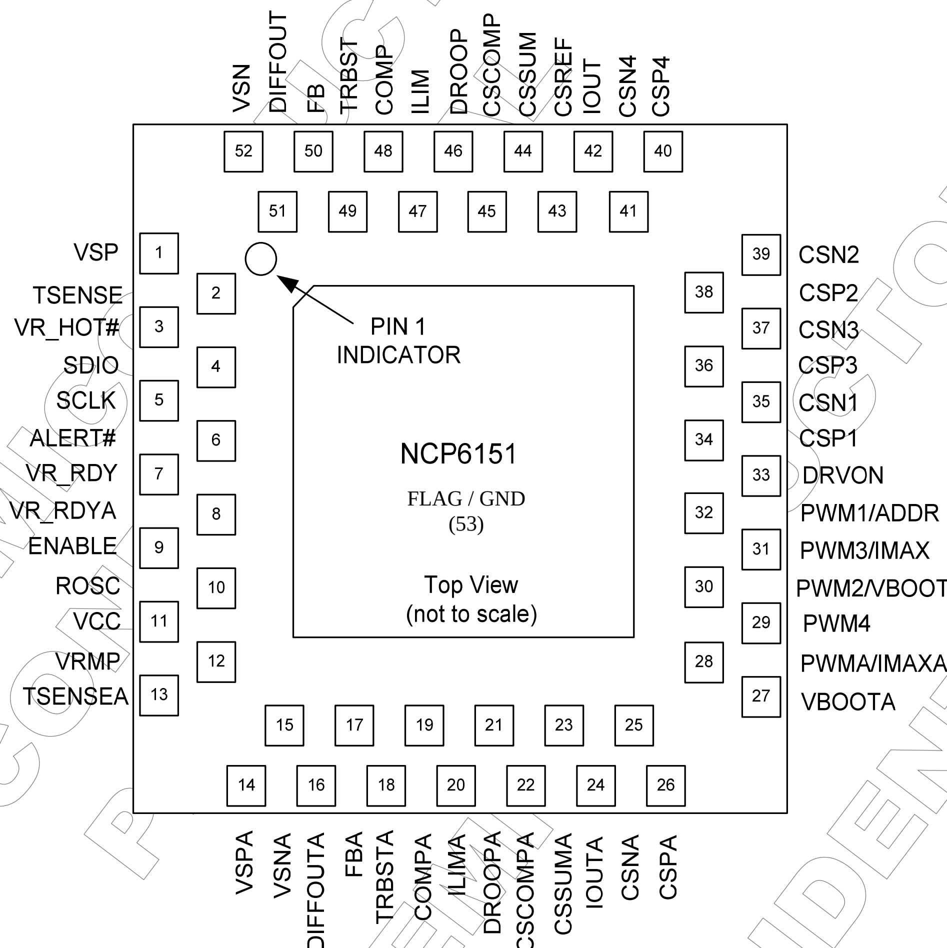
Applications

- Desktop & Notebook Processors

Block Diagram



NCP6151 QFN52 Dual Row Pin Diagram

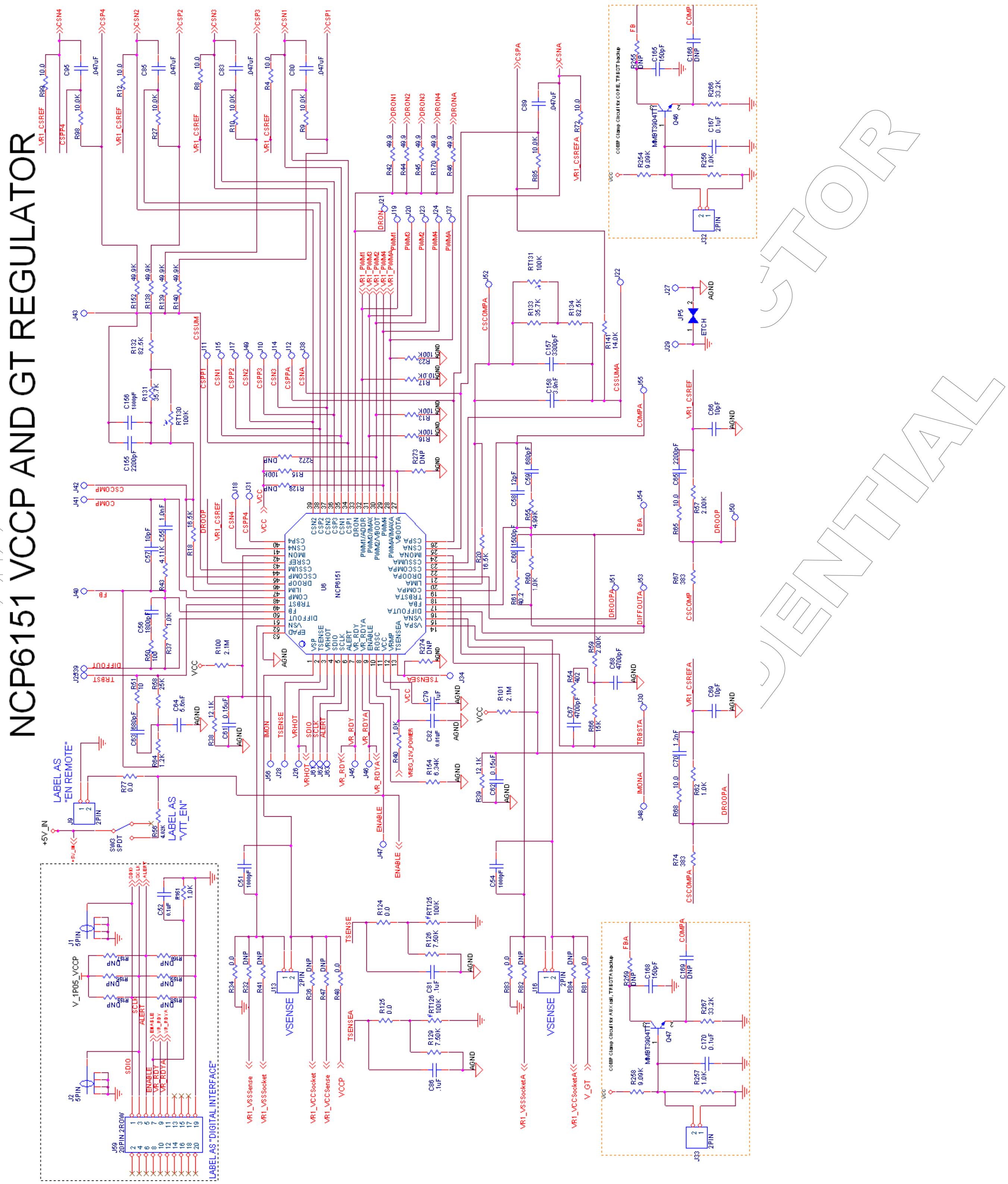


NCP6151/NCP6151A QFN52 Dual Row Pin List and Descriptions

Pin No.	Symbol	Description
1	VSP	Non-inverting input to the core differential remote sense amplifier.
2	TSENSE	Temp Sense input for the multiphase converter
3	VR_HOT#	Thermal logic output for over temperature.
4	SDIO	Serial VID data interface.
5	SCLK	Serial VID clock.
6	ALERT#	Serial VID ALERT#.
7	VR_RDY	Open drain output. High indicates that the core output is regulating.
8	VR_RDYA	Open drain output. High indicates that the aux output is regulating.
9	ENABLE	Logic input. Logic high enables both outputs and logic low disables both outputs.
10	ROSC	A resistance from this pin to ground programs the oscillator frequency. This pin supplies a trimmed output voltage of 2V.
11	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground.
12	VRMP	Feed-forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control of the ramp of PWM slope
13	TSENSEA	Temp sense for the single phase converter

14	VSPA	Non-inverting input to the aux differential remote sense amplifier
15	VSNA	Inverting input to the aux differential remote sense amplifier
16	DIFFOUTA	Output of the aux differential remote sense amplifier
17	FBA	Error amplifier voltage feedback for aux output
18	TRBSTA	Compensation pin for the load transient boost.
19	COMPA	Output of the aux error amplifier and the inverting input of the PWM comparator for aux output
20	ILIMA	Over current shutdown threshold setting for aux output. A resistor to CSCOMPA sets the threshold.
21	DROOPA	Used to program droop function for aux output. It's connected to the resistor divider placed between CSCOMPA and CSREFA.
22	CSCOMPA	Output of total current sense amplifier for aux output
23	CSSUMA	Inverting input of total current sense amplifier for aux output
24	IOUTA	Total output current monitor for aux output
25	CSNA	Inverting input to aux current sense amplifier
26	CSPA	Non-Inverting input to aux current sense amplifier
27	VBOOTA	VBOOTA Voltage input pin. Set to adjust the aux boot-up voltage
28	PWMA/IMAXA	Aux PWM output to gate driver. During start up it is used to program ICC_MAXA with a resistor to ground
29	PWM4	Phase 4 PWM output. Pull to VCC to program 3 phase operation.
30	PWM2/VBOOT	Phase 2 PWM output. VBoot program pin. During start up it is used to program VBOOT with a resistor to ground.
31	PWM3/IMAX	Phase 3 PWM output. ICC_MAX Input Pin. During start up it is used to program ICC_MAX with a resistor to ground.
32	PWM1/ADDR	Phase 1 PWM output. A resistor to ground on this pin programs the SVID address of the devise.
33	DRON	Bidirectional gate drive enable for core output.
34	CSP1	Non-inverting input to current balance sense amplifier for phase 1
35	CSN1	Inverting input to current balance sense amplifier for phase 1
36	CSP3	Non-inverting input to current balance sense amplifier for phase 3
37	CSN3	Inverting input to current balance sense amplifier for phase 3
38	CSP2	Non-inverting input to current balance sense amplifier for phase 2
39	CSN2	Inverting input to current balance sense amplifier for phase 2
40	CSP4	Non-inverting input to current balance sense amplifier for phase 4
41	CSN4	Inverting input to current balance sense amplifier for phase 4
42	IOUT	Total output current monitor for core output.
43	CSREF	Total output current sense amplifier reference voltage input.
44	CSSUM	Inverting input of total current sense amplifier for core output.
45	CSCOMP	Output of total current sense amplifier for core output.
46	DROOP	Used to program droop function for core output. It's connected to the resistor divider placed between CSCOMP and CSREF summing node.
47	ILIM	Over current shutdown threshold setting for core output. Resistor to CSCOMP to set threshold.
48	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators for the core output.
49	TRBST	Compensation pin for the load transient boost.
50	FB	Error amplifier voltage feedback for core output
51	DIFFOUT	Output of the core differential remote sense amplifier.
52	VSN	Inverting input to the core differential remote sense amplifier.
53	FLAG / GND	Power supply return (QFN Flag)

Four Phase Plus One Phase Application Control Circuit



ABSOLUTE MAXIMUM RATINGS

Electrical Information

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP,COMPA	VCC+0.3V	-0.3V	2mA	2mA
CSCOMP, CSCOMPA	VCC+0.3V	-0.3V	2mA	2mA
VSN	GND+300mV	GND–300mV	1mA	1mA
DIFFOUT, DIFFOUTA	VCC+0.3V	-0.3V	2mA	2mA
VR_RDY,VR_RDYA	VCC+0.3V	-0.3V	N/A	2mA
VCC	6.5V	-0.3V	N/A	N/A
ROSC	VCC+0.3V	-0.3V	1mA	N/A
IOUT, IOUTA Output	2.0 V	-0.3V		
VRMP	+25V	-0.3V		
All Other Pins	VCC+0.3V	-0.3 V		

***All signals referenced to GND unless noted otherwise.**

Thermal Information

Thermal Characteristic QFN Package [2]	$R_{\square JA}$	TBD	°C/W
Operating Junction Temperature Range[3]	T_J	-10 to 125	°C
Operating Ambient Temperature Range		-10 to 100	°C
Maximum Storage Temperature Range	T_{STG}	- 40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

*The maximum package power dissipation must be observed.

2) JESD 51-5 (1S2P Direct-Attach Method) with 0 LFM

3) JESD 51-7 (1S2P Direct-Attach Method) with 0 LFM

NCP6151/NCP6151A(4+1) ELECTRICAL CHARACTERISTICS

Unless otherwise stated: $-10^oC<T_A<100^oC$; 4.75 V<VCC<5.25V; C_{VCC}=0.1μF

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
Input Bias Current	@ 1.3V	-400		400	nA
Open Loop DC Gain	CL = 20pF to GND, RL = 10KΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20pF to GND, RL = 10KΩ to GND		60		MHz
Slew Rate	**ΔVin = 100mV, G = -10V/V,** ΔVout = 1.5V – 2.5V, CL = 20pF to GND, DC Load = 10k to GND		20		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0mA	3.5	-	-	V
Minimum Output Voltage	I_{SINK} = 2.0mA	-	-	1	V
Differential Summing Amplifier					
Input Bias Current		-400	-	400	nA
VSP Input Voltage Range		-0.3	-	3.0	V
VSN Input Voltage Range		-0.3	-	0.3	V
-3dB Bandwidth	CL = 20pF to GND, RL = 10KΩ to GND		12		MHz
Closed Loop DC gain VS to Diffout	VS+ to VS- = 0.5 to 1.3V		1.0		V/V
Droop Accuracy	CSREF-DROOP=80mV DAC=0.8V to 1.2V	-81.5		-78.5	mV
Maximum Output Voltage	I_{SOURCE} = 2mA	3.0	-	-	V
Minimum Output Voltage	I_{SINK} = 2mA	-	-	0.5	V

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated: -10°C<T_A<100°C; 4.75V<VCC<5.25V; C_{VCC}=0.1µF

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos)		-300		300	uV
Input Bias Current	CSSUM=CSREF= 1V	-7.5		7.5	nA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20pF to GND, R_L = 10KΩ to GND		9		MHz
Maximum CSCOMP (A) Output Voltage	Isource = 2mA	3.5	-	-	V
Minimum CSCOMP(A) Output Voltage	Isink = 500uA	-	-	0.1	V
CURRENT BALANCE AMPLIFIER					
Input Bias Current	CSPx=CSNx=1.2V	-50	-	50	nA
Common Mode Input Voltage Range	CSPx=CSNx	0	-	2.0	V
Differential Mode Input Voltage Range	CSNx=1.2V	-100	-	100	mV
Closed loop Input Offset Voltage Matching	CSPx=CSNx =1.2V, Measured from the average	-1.5	-	1.5	mV
Current Sense Amplifier Gain	0V < CSPx-CSNx < 0.1V,	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSN=CSP=10mV to 30mV	-3		3	%
-3dB Bandwidth			8		MHz
INPUT SUPPLY					
VCC Quiescent Current	EN=high	TBD	35	TBD	mA
	EN=low		TBD	TBD	µA
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4.1			V
VCC UVLO Hysteresis			200		mV
DAC SLEW RATE					
Soft Start Slew Rate			TBD		mv/us
Slew Rate Slow			5		mv/us
Slew Rate Fast			20		mv/us
AUX Soft Start Slew Rate			TBD		mv/us
AUX Slew Rate Slow			2.5		mv/us
AUX Slew Rate Fast			10		mv/us
ENABLE INPUT					
Enable High Input Leakage Current	External 1K pull-up to 3.3V	-		1.0	µA
Upper Threshold	V_{UPPER}	0.8			V
Lower Threshold	V_{LOWER}			0.4	V
Total Hysteresis	$V_{UPPER} - V_{LOWER}$		20		mV
Enable Delay Time	Measure time from Enable transitioning HI to when DRON goes high, Vboot is not 0V			5.0	ms

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated: $-10^oC<T_A<100^oC$; 4.75V<VCC<5.25V;C_{VCC}=0.1μF

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DRVON					
Output High Voltage	Sourcing 500uA	3.5			V
Output Low Voltage	Sinking 500uA			0.1	V
Rise/Fall Time	CL (PCB) = 20pF, ΔVo = 10% to 90%	-	10		ns
Internal Pull Down Resistance	EN = Low		70		kΩ
IOUT / IOUTA OUTPUT					
Input Referred Offset Voltage	I_{limit} to CSREF	-1		1	mV
Output Source Current	Ilimit sink current= 80uA			800	uA
Current Gain	$(IOUT_{CURRENT})$ / $(ILIMIT_{CURRENT})$, R_{ILIM} = 20k, R_{IOUT} = 5.0k , Temp range: 0 °C to 60 °C	9.5	10	10.5	
OSCILLATOR					
Switching Frequency Range		200	-	1000	KHz
Switching Frequency Accuracy	250KHz < Fsw < 1MHz	-10	-	10	%
4 Phase Operation	R_T=6.98 kΩ	310	350	390	kHz
Rosc Output Voltage	R_T=6.98 kΩ	1.95	2.00	2.05	V
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft-Start		2.175	2.2	2.225	V
Over Voltage Threshold Above DAC	VSP(A) rising	150	175	200	mV
Over Voltage Delay	VSP(A) rising to PWMx low		50		ns
Overvoltage Hysteresis	VSP(A) falling		25		mV
Under Voltage Threshold Below DAC-DROOP	VSP(A) falling	250	300	350	mV
Under-voltage Hysteresis	VSP(A) rising		25		mV
Under-voltage Delay			5		us
VR12 DAC					
System Voltage Accuracy	1.0 V ≤ DAC < 1.52 V 0.8V< DAC < 0.995 V 0.25V < DAC < 0.795 V	-0.5 -5 -8		0.5 5 8	% mV mV mV
Droop Feed-Forward Current	Measure on DROOP pin	60	66	72	μA
Droop Feed-Forward Pulse On-Time			0.16		μs
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shutdown after 50 us delay)	(PS0) Rlim=20k	9.0	10	11.0	μA
ILIM Threshold Current (immediate OCP shutdown)	(PS0) Rlim=20k	13.5	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 us delay)	(PS1, PS2, PS3) Rlim=20k	TBD	10	TBD	μA
ILIM Threshold Current (immediate OCP shutdown)	(PS1, PS2, PS3) Rlim=20k	TBD	15	TBD	μA
Over-Current (DCR) Threshold	During startup, CSP-CSN	36	48	60	mV
Maximum Timer for OCP shutdown			-	55	μs
CSCOMP OCP Threshold			50		mV

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated: $-10^oC<T_A<100^oC$; $4.75V<VCC<5.25V$; $C_{VCC}=0.1\mu F$

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
MODULATORS (PWM COMPARATORS) FOR CORE & AUX					
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3	-	V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI VRMP=12.0V	-	2.5	-	V
PWM Ramp Duty Cycle Matching	COMP=2V, PWM Ton matching		.75		%
PWM Phase Angle Error	Between adjacent phases	-10		10	deg
Ramp Feed-forward Voltage range		5		20	V
TRBST					
Output Low Voltage	I_{Sink}= 500uA			TBD	mV
TRBSTA					
Output Low Voltage	I_{Sink}= 500uA			TBD	mV
VR_HOT#					
Output Low Voltage	$I_{\_VRHOT}$ = -4mA			0.3	V
Output Leakage Current	High Impedance State	-1.0	-	1.0	µA
TSENSE/TSENSEA					
Alert# Assert Threshold	NTC=100k in parallel with 8.2k =97C		483		mV
Alert# De-assert Threshold	NTC=100k in parallel with 8.2k =94C		503		mV
VRHOT Assert Threshold	NTC=100k in parallel with 8.2k =100C		462		mV
VRHOT Rising Threshold	NTC=100k in parallel with 8.2k =97C		483		mV
TSENSE Bias Current		117.6	120	122.4	µA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		-1		+1	%
Differential Nonlinearity (DNL)	8-bit			1	LSB
Power Supply Sensitivity			+/-1		%
Conversion Time			30		µs
Round Robin			90		µs
VR_RDY, VR_RDYA (POWER GOOD)	**OUTPUT**				
Output Low Saturation Voltage	$I_{VR\_RDY(A)}$ = 4mA,	-	-	0.3	V
Rise Time	External pull-up of 1KΩ to 3.3V, C_{TOT} = 45pF, ΔVo = 10% to 90%	-	100		ns
Fall Time	External pull-up of 1KΩ to 3.3V, C_{TOT} = 45pF, ΔVo = 90% to 10%		10		ns
Output Voltage at Power-up	VR_RDY, VR_RDYA pulled up to 5V via 2KΩ	-	-	1.0	V
Output Leakage Current When High	VR_RDY & VR_RDYA = 5.0V	-1.0	-	1.0	µA
VR_RDY Delay (rising)	DAC=TARGET to VR_RDY		500		µs
VR_RDY Delay (falling)	From OCP or OVP	-	5	-	µs
PWM Outputs					
Output High Voltage	Sourcing 500uA	VCC – 0.1V	-	-	V
Output Mid Voltage	No Load, SetPS=02	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500uA	-	-	0.7	V
Rise and Fall Time	CL (PCB) = 50pF, ΔVo = GND to VCC	-	10		ns
Phase Detection					
PWM Pin Source Current			100		µA
PWM Pin Threshold Voltage			3.3		V
Phase Detect Timer			50		µs
VRMP UVLO					
UVLO Threshold	VRMP rising			TBD	V
	VRMP falling	TBD			V
VRMP UVLO Hysteresis			200		mV

SCLK, SDIO					

V_{IL}	Input Low Voltage			.45	V
V_{IH}	Input High Voltage	.65			V
V_{HYS}	Hysteresis Voltage	50			mV
V_{OH}	Output High Voltage		1.05		V
V_{OL}	Output Low Voltage (SDIO only)		TBD		mV

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated: $-10^oC<T_A<100^oC$; 4.75V<VCC<5.25V; $C_{VCC}=0.1\mu F$

Parameter	Test Condition	MIN	TYP	MAX	Units
R_{ON}	Buffer On Resistance (data line, ALERT#, and VRHOT)	4		13	Ω
Leakage Current		-100		100	µA
Pad Capacitance				4.0	pF
VR clock to data delay (Tco)		4		8.3	ns
Setup time (Tsu)		7			ns
Hold time (Thld)		14			ns

Table 2: VR12 VID Codes

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	OFF	00
0	0	0	0	0	0	0	1	0.25000	01
0	0	0	0	0	0	1	0	0.25500	02
0	0	0	0	0	0	1	1	0.26000	03
0	0	0	0	0	1	0	0	0.26500	04
0	0	0	0	0	1	0	1	0.27000	05
0	0	0	0	0	1	1	0	0.27500	06
0	0	0	0	0	1	1	1	0.28000	07
0	0	0	0	1	0	0	0	0.28500	08
0	0	0	0	1	0	0	1	0.29000	09
0	0	0	0	1	0	1	0	0.29500	0A
0	0	0	0	1	0	1	1	0.30000	0B
0	0	0	0	1	1	0	0	0.30500	0C
0	0	0	0	1	1	0	1	0.31000	0D
0	0	0	0	1	1	1	0	0.31500	0E
0	0	0	0	1	1	1	1	0.32000	0F
0	0	0	1	0	0	0	0	0.32500	10
0	0	0	1	0	0	0	1	0.33000	11
0	0	0	1	0	0	1	0	0.33500	12
0	0	0	1	0	0	1	1	0.34000	13
0	0	0	1	0	1	0	0	0.34500	14
0	0	0	1	0	1	0	1	0.35000	15
0	0	0	1	0	1	1	0	0.35500	16
0	0	0	1	0	1	1	1	0.36000	17
0	0	0	1	1	0	0	0	0.36500	18
0	0	0	1	1	0	0	1	0.37000	19
0	0	0	1	1	0	1	0	0.37500	1A
0	0	0	1	1	0	1	1	0.38000	1B
0	0	0	1	1	1	0	0	0.38500	1C
0	0	0	1	1	1	0	1	0.39000	1D
0	0	0	1	1	1	1	0	0.39500	1E
0	0	0	1	1	1	1	1	0.40000	1F
0	0	1	0	0	0	0	0	0.40500	20
0	0	1	0	0	0	0	1	0.41000	21
0	0	1	0	0	0	1	0	0.41500	22
0	0	1	0	0	0	1	1	0.42000	23
0	0	1	0	0	1	0	0	0.42500	24
0	0	1	0	0	1	0	1	0.43000	25
0	0	1	0	0	1	1	0	0.43500	26

Table 2: VR12 VID Codes (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	0	1	1	1	0.44000	27
0	0	1	0	1	0	0	0	0.44500	28
0	0	1	0	1	0	0	1	0.45000	29
0	0	1	0	1	0	1	0	0.45500	2A
0	0	1	0	1	0	1	1	0.46000	2B
0	0	1	0	1	1	0	0	0.46500	2C
0	0	1	0	1	1	0	1	0.47000	2D
0	0	1	0	1	1	1	0	0.47500	2E
0	0	1	0	1	1	1	1	0.48000	2F
0	0	1	1	0	0	0	0	0.48500	30
0	0	1	1	0	0	0	1	0.49000	31
0	0	1	1	0	0	1	0	0.49500	32
0	0	1	1	0	0	1	1	0.50000	33
0	0	1	1	0	1	0	0	0.50500	34
0	0	1	1	0	1	0	1	0.51000	35
0	0	1	1	0	1	1	0	0.51500	36
0	0	1	1	0	1	1	1	0.52000	37
0	0	1	1	1	0	0	0	0.52500	38
0	0	1	1	1	0	0	1	0.53000	39
0	0	1	1	1	0	1	0	0.53500	3A
0	0	1	1	1	0	1	1	0.54000	3B
0	0	1	1	1	1	0	0	0.54500	3C
0	0	1	1	1	1	0	1	0.55000	3D
0	0	1	1	1	1	1	0	0.55500	3E
0	0	1	1	1	1	1	1	0.56000	3F
0	1	0	0	0	0	0	0	0.56500	40
0	1	0	0	0	0	0	1	0.57000	41
0	1	0	0	0	0	1	0	0.57500	42
0	1	0	0	0	0	1	1	0.58000	43
0	1	0	0	0	1	0	0	0.58500	44
0	1	0	0	0	1	0	1	0.59000	45
0	1	0	0	0	1	1	0	0.59500	46
0	1	0	0	0	1	1	1	0.60000	47
0	1	0	0	1	0	0	0	0.60500	48
0	1	0	0	1	0	0	1	0.61000	49
0	1	0	0	1	0	1	0	0.61500	4A
0	1	0	0	1	0	1	1	0.62000	4B
0	1	0	0	1	1	0	0	0.62500	4C
0	1	0	0	1	1	0	1	0.63000	4D
0	1	0	0	1	1	1	0	0.63500	4E
0	1	0	0	1	1	1	1	0.64000	4F
0	1	0	1	0	0	0	0	0.64500	50
0	1	0	1	0	0	0	1	0.65000	51
0	1	0	1	0	0	1	0	0.65500	52
0	1	0	1	0	0	1	1	0.66000	53
0	1	0	1	0	1	0	0	0.66500	54
0	1	0	1	0	1	0	1	0.67000	55
0	1	0	1	0	1	1	0	0.67500	56
0	1	0	1	0	1	1	1	0.68000	57
0	1	0	1	1	0	0	0	0.68500	58

Table 2: VR12 VID Codes (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	1	1	0	0	1	0.69000	59
0	1	0	1	1	0	1	0	0.69500	5A
0	1	0	1	1	0	1	1	0.70000	5B
0	1	0	1	1	1	0	0	0.70500	5C
0	1	0	1	1	1	0	1	0.71000	5D
0	1	0	1	1	1	1	0	0.71500	5E
0	1	0	1	1	1	1	1	0.72000	5F
0	1	1	0	0	0	0	0	0.72500	60
0	1	1	0	0	0	0	1	0.73000	61
0	1	1	0	0	0	1	0	0.73500	62
0	1	1	0	0	0	1	1	0.74000	63
0	1	1	0	0	1	0	0	0.74500	64
0	1	1	0	0	1	0	1	0.75000	65
0	1	1	0	0	1	1	0	0.75500	66
0	1	1	0	0	1	1	1	0.76000	67
0	1	1	0	1	0	0	0	0.76500	68
0	1	1	0	1	0	0	1	0.77000	69
0	1	1	0	1	0	1	0	0.77500	6A
0	1	1	0	1	0	1	1	0.78000	6B
0	1	1	0	1	1	0	0	0.78500	6C
0	1	1	0	1	1	0	1	0.79000	6D
0	1	1	0	1	1	1	0	0.79500	6E
0	1	1	0	1	1	1	1	0.80000	6F
0	1	1	1	0	0	0	0	0.80500	70
0	1	1	1	0	0	0	1	0.81000	71
0	1	1	1	0	0	1	0	0.81500	72
0	1	1	1	0	0	1	1	0.82000	73
0	1	1	1	0	1	0	0	0.82500	74
0	1	1	1	0	1	0	1	0.83000	75
0	1	1	1	0	1	1	0	0.83500	76
0	1	1	1	0	1	1	1	0.84000	77
0	1	1	1	1	0	0	0	0.84500	78
0	1	1	1	1	0	0	1	0.85000	79
0	1	1	1	1	0	1	0	0.85500	7A
0	1	1	1	1	0	1	1	0.86000	7B
0	1	1	1	1	1	0	0	0.86500	7C
0	1	1	1	1	1	0	1	0.87000	7D
0	1	1	1	1	1	1	0	0.87500	7E
0	1	1	1	1	1	1	1	0.88000	7F
1	0	0	0	0	0	0	0	0.88500	80
1	0	0	0	0	0	0	1	0.89000	81
1	0	0	0	0	0	1	0	0.89500	82
1	0	0	0	0	0	1	1	0.90000	83
1	0	0	0	0	1	0	0	0.90500	84
1	0	0	0	0	1	0	1	0.91000	85
1	0	0	0	0	1	1	0	0.91500	86
1	0	0	0	0	1	1	1	0.92000	87
1	0	0	0	1	0	0	0	0.92500	88
1	0	0	0	1	0	0	1	0.93000	89
1	0	0	0	1	0	1	0	0.93500	8A
1	0	0	0	1	0	1	1	0.94000	8B

Table 2: VR12 VID Codes (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	0	0	1	1	0	0	0.94500	8C
1	0	0	0	1	1	0	1	0.95000	8D
1	0	0	0	1	1	1	0	0.95500	8E
1	0	0	0	1	1	1	1	0.96000	8F
1	0	0	1	0	0	0	0	0.96500	90
1	0	0	1	0	0	0	1	0.97000	91
1	0	0	1	0	0	1	0	0.97500	92
1	0	0	1	0	0	1	1	0.98000	93
1	0	0	1	0	1	0	0	0.98500	94
1	0	0	1	0	1	0	1	0.99000	95
1	0	0	1	0	1	1	0	0.99500	96
1	0	0	1	0	1	1	1	1.00000	97
1	0	0	1	1	0	0	0	1.00500	98
1	0	0	1	1	0	0	1	1.01000	99
1	0	0	1	1	0	1	0	1.01500	9A
1	0	0	1	1	0	1	1	1.02000	9B
1	0	0	1	1	1	0	0	1.02500	9C
1	0	0	1	1	1	0	1	1.03000	9D
1	0	0	1	1	1	1	0	1.03500	9E
1	0	0	1	1	1	1	1	1.04000	9F
1	0	1	0	0	0	0	0	1.04500	A0
1	0	1	0	0	0	0	1	1.05000	A1
1	0	1	0	0	0	1	0	1.05500	A2
1	0	1	0	0	0	1	1	1.06000	A3
1	0	1	0	0	1	0	0	1.06500	A4
1	0	1	0	0	1	0	1	1.07000	A5
1	0	1	0	0	1	1	0	1.07500	A6
1	0	1	0	0	1	1	1	1.08000	A7
1	0	1	0	1	0	0	0	1.08500	A8
1	0	1	0	1	0	0	1	1.09000	A9
1	0	1	0	1	0	1	0	1.09500	AA
1	0	1	0	1	0	1	1	1.10000	AB
1	0	1	0	1	1	0	0	1.10500	AC
1	0	1	0	1	1	0	1	1.11000	AD
1	0	1	0	1	1	1	0	1.11500	AE
1	0	1	0	1	1	1	1	1.12000	AF
1	0	1	1	0	0	0	0	1.12500	B0
1	0	1	1	0	0	0	1	1.13000	B1
1	0	1	1	0	0	1	0	1.13500	B2
1	0	1	1	0	0	1	1	1.14000	B3
1	0	1	1	0	1	0	0	1.14500	B4

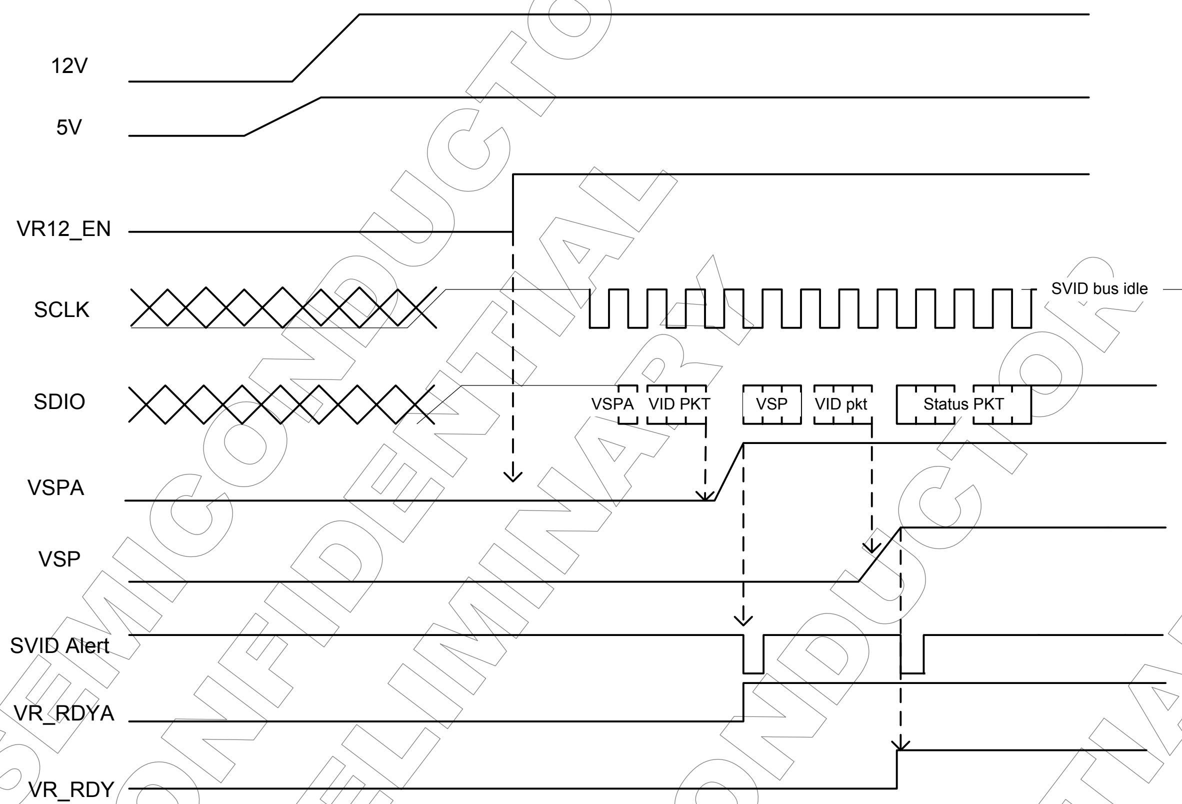
Table 2: VR12 VID Codes (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	1	0	1	0	1	1.15000	B5
1	0	1	1	0	1	1	0	1.15500	B6
1	0	1	1	0	1	1	1	1.16000	B7
1	0	1	1	1	0	0	0	1.16500	B8
1	0	1	1	1	0	0	1	1.17000	B9
1	0	1	1	1	0	1	0	1.17500	BA
1	0	1	1	1	0	1	1	1.18000	BB
1	0	1	1	1	1	0	0	1.18500	BC
1	0	1	1	1	1	0	1	1.19000	BD
1	0	1	1	1	1	1	0	1.19500	BE
1	0	1	1	1	1	1	1	1.20000	BF
1	1	0	0	0	0	0	0	1.20500	C0
1	1	0	0	0	0	0	1	1.21000	C1
1	1	0	0	0	0	1	0	1.21500	C2
1	1	0	0	0	0	1	1	1.22000	C3
1	1	0	0	0	1	0	0	1.22500	C4
1	1	0	0	0	1	0	1	1.23000	C5
1	1	0	0	0	1	1	0	1.23500	C6
1	1	0	0	0	1	1	1	1.24000	C7
1	1	0	0	1	0	0	0	1.24500	C8
1	1	0	0	1	0	0	1	1.25000	C9
1	1	0	0	1	0	1	0	1.25500	CA
1	1	0	0	1	0	1	1	1.26000	CB
1	1	0	0	1	1	0	0	1.26500	CC
1	1	0	0	1	1	0	1	1.27000	CD
1	1	0	0	1	1	1	0	1.27500	CE
1	1	0	0	1	1	1	1	1.28000	CF
1	1	0	1	0	0	0	0	1.28500	D0
1	1	0	1	0	0	0	1	1.29000	D1
1	1	0	1	0	0	1	0	1.29500	D2
1	1	0	1	0	0	1	1	1.30000	D3
1	1	0	1	0	1	0	0	1.30500	D4
1	1	0	1	0	1	0	1	1.31000	D5
1	1	0	1	0	1	1	0	1.31500	D6
1	1	0	1	0	1	1	1	1.32000	D7
1	1	0	1	1	0	0	0	1.32500	D8
1	1	0	1	1	0	0	1	1.33000	D9
1	1	0	1	1	0	1	0	1.33500	DA
1	1	0	1	1	0	1	1	1.34000	DB
1	1	0	1	1	1	0	0	1.34500	DC
1	1	0	1	1	1	0	1	1.35000	DD

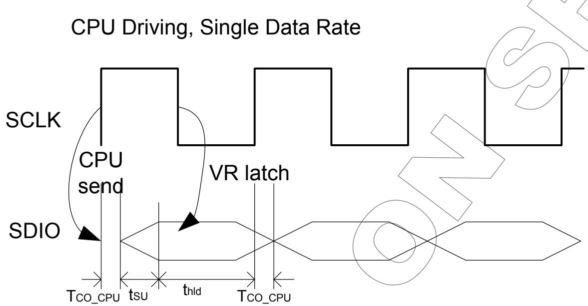
Table 2: VR12 VID Codes (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	0	1	1	1	1	0	1.35500	DE
1	1	0	1	1	1	1	1	1.36000	DF
1	1	1	0	0	0	0	0	1.36500	E0
1	1	1	0	0	0	0	1	1.37000	E1
1	1	1	0	0	0	1	0	1.37500	E2
1	1	1	0	0	0	1	1	1.38000	E3
1	1	1	0	0	1	0	0	1.38500	E4
1	1	1	0	0	1	0	1	1.39000	E5
1	1	1	0	0	1	1	0	1.39500	E6
1	1	1	0	0	1	1	1	1.40000	E7
1	1	1	0	1	0	0	0	1.40500	E8
1	1	1	0	1	0	0	1	1.41000	E9
1	1	1	0	1	0	1	0	1.41500	EA
1	1	1	0	1	0	1	1	1.42000	EB
1	1	1	0	1	1	0	0	1.42500	EC
1	1	1	0	1	1	0	1	1.43000	ED
1	1	1	0	1	1	1	0	1.43500	EE
1	1	1	0	1	1	1	1	1.44000	EF
1	1	1	1	0	0	0	0	1.44500	F0
1	1	1	1	0	0	0	1	1.45000	F1
1	1	1	1	0	0	1	0	1.45500	F2
1	1	1	1	0	0	1	1	1.46000	F3
1	1	1	1	0	1	0	0	1.46500	F4
1	1	1	1	0	1	0	1	1.47000	F5
1	1	1	1	0	1	1	0	1.47500	F6
1	1	1	1	0	1	1	1	1.48000	F7
1	1	1	1	1	0	0	0	1.48500	F8
1	1	1	1	1	0	0	1	1.49000	F9
1	1	1	1	1	0	1	0	1.49500	FA
1	1	1	1	1	0	1	1	1.50000	FB
1	1	1	1	1	1	0	0	1.50500	FC
1	1	1	1	1	1	0	1	1.51000	FD
1	1	1	1	1	1	1	0	1.51500	FE
1	1	1	1	1	1	1	1	1.52000	FF

Start Up Timing Diagram



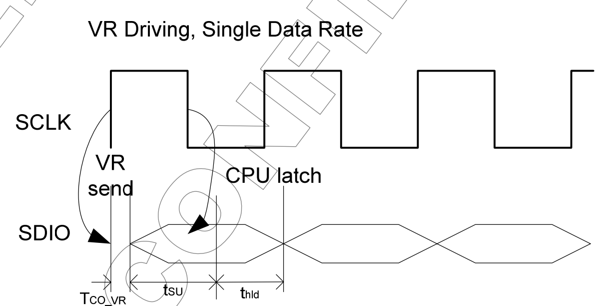
SVID Timing Diagram



T_{co_CPU} = clock to data delay in CPU

$tsu = 0.5*T - T_{co\_CPU}$

$thld = 0.5*T + T_{co\_CPU}$



T_{co_VR} = clock to data delay in VR

$tsu = T - 2*T_{fly} - T_{co\_VR}$

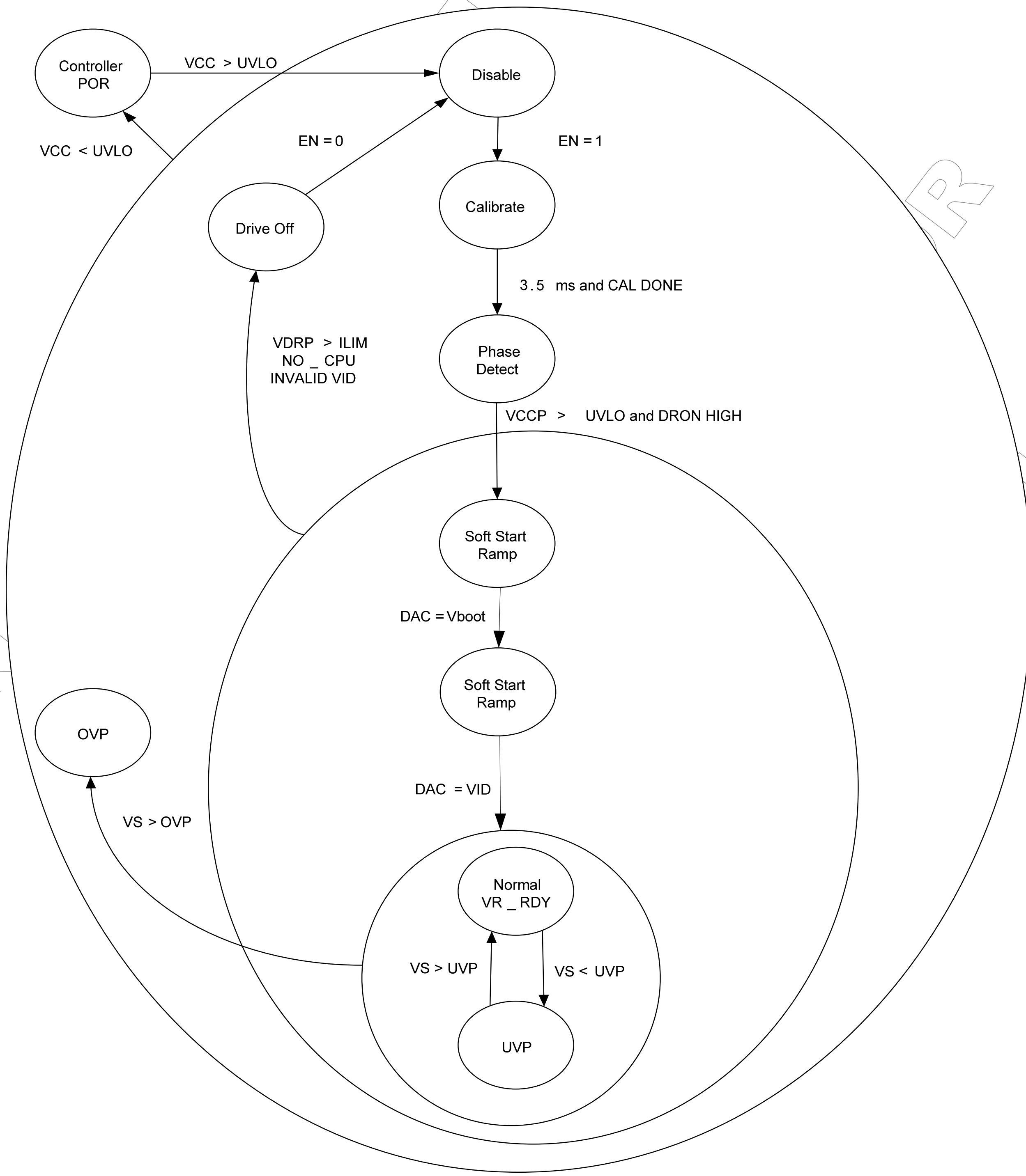
$thld = 2*T_{fly} + T_{co\_VR}$

T_{fly} propagation time on Serial VID bus

State Truth Table

STATE	VR_RDY(A) Pin	Error AMP Comp(A) Pin	OVP(A) & UVP(A)	DRVON PIN	Method of Reset
POR 0<VCC<UVLO	N/A	N/A	N/A	Resistive pull down	
Disabled EN < threshold UVLO >threshold	Low	Low	Disabled	Low	
Start up Delay & Calibration EN> threshold UVLO>threshold	Low	Low	Disabled	Low	
DRVON Fault EN> threshold UVLO>threshold DRVON<threshold	Low	Low	Disabled	Resistive pull up	Driver must release DRVON to high
Soft Start EN > threshold UVLO >threshold DRVON > High	Low	Operational	Active / No latch	High	
Normal Operation EN > threshold UVLO >threshold DRVON > High	High	Operational	Active / Latching	High	N/A
Over Voltage	Low	N/A	DAC+150mV	High	
Over Current	Low	Operational	Last DAC Code	Low	
VID Code = 00h	Low	Low	Disabled	High, PWM outputs in mid state	Set Valid VID Code

State Diagram



General

The NCP6151/NCP6151A is a dual output four phase plus one phase dual edge modulated multiphase PWM controller designed to meet the Intel VR12 specifications with a serial SVID control interface. The NCP6151/NCP6151A implements PS0, PS1, PS2 and PS3 power saving states. NCP6151A support coupled inductor operation. It operates with 2 phases versus NCP6151 operating with single phase during PS1 mode.

For NCP6151 Core Rail:

Power Status	PWM Output Operating Mode
PS0	Multi-phase PWM interleaving output
PS1	Single-phase RPM CCM mode (PWM1 only, PWM2~4 stay in Mid)
PS2	Single-phase RPM DCM mode (PWM1 only, PWM2~4 stay in Mid)
PS3	Existing definition is same as PS2

For NCP6151A Core Rail:

Power Status	PWM Output Operating Mode
PS0	Multi-phase PWM interleaving output
PS1	Two Phase PWM1 & PWM3
PS2	RPM PWM1 with sync diode behavior on PWM3
PS3	Existing definition is same as PS2

For NCP6151/NCP6151A AUX Rail:

Power Status	PWM Output Operating Mode
PS0	Single-phase RPM output
PS1	Same as PS0
PS2	Single-phase RPM DCM mode
PS3	Existing definition is same as PS2

For NCP6151/NCP6151A, VID code change is supported by SVID interface with three options as below:

Option	SVID Command Code	Feature	Register Address (Indicating the slew rate of VID code change)
SetVID_Fast	01h	>10mV/us VID code change slew rate	24h
SetVID_Slow	02h	=1/4 of SetVID_Fast VID code change slew rate	25h
SetVID_Decay	03h	No control, VID code down	N/A

Serial VID

The NCP6151/NCP6151A supports the Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#). The table of supported registers is shown below.

Index	Name	Description	Access	Default
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah	R	0x1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	R	0x00
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R	0x03
05h	Protocol ID	Identifies the SVID Protocol the NCP6151 supports	R	0x01
06h	Capability	Informs the Master of the NCP6151's Capabilities, 1 = supported, 0 = not supported Bit 7 = Iout_format. Bit 7 = 0 when 1A = 1LSB of Reg	R	0xC7

		15h. Bit 7 = 1 when Reg 15 FFh = Icc_Max. Default = 1 Bit 6 = ADC Measurement of Temp Supported = 1 Bit 5 = ADC Measurement of Pin Supported = 0 Bit 4 = ADC Measurement of Vin Supported = 0 Bit 3 = ADC Measurement of Iin Supported = 0 Bit 2 = ADC Measurement of Pout Supported = 1 Bit 1 = ADC Measurement of Vout Supported = 1 Bit 0 = ADC Measurement of Iout Supported = 1		
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR.	R	00h
11h	Status_2	Data register showing optional status_2 data.	R	00h
12h	Temp zone	Data register showing temperature zones the system is operating in	R	00h
15h	I_out	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max	R	01h
16h	V_out	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 8mV	R	01h
17h	VR_Temp	8 bit binary word ADC of voltage. Binary format in deg C, IE 100C=64h. A value of 00h indicates this function is not supported	R	01h
18h	P_out	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported	R	01h
1Ch	Status 2 Last read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h
21h	Icc_Max	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.	R	00h
22h	Temp_Max	Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 100°C and programmable over the SVID Interface	R/W	64h
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/us.	R	0Ah
25h	SR_slow	Slew Rate for SetVID_slow commands. It is 4X slower than the SR_fast rate. Binary format in mV/us	R	02h
26h	Vboot	The Vboot is programmed using resistors on the Vboot pin which is sensed on power up. The NCP6151 will ramp to Vboot and hold at Vboot until it receives a new SVID SetVID command to move to a different voltage. Default value=0, i.e. this occurs if no resistor is connected to the Vboot pin. IN this case the NCP6151 will wait till it gets an SVID command to set the output voltage., VR12 VID format, IE 97h=1.0Volts	R	00h
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. VR 12 VID format.	RW	FBh
31h	VID setting	Data register containing currently programmed VID voltage. VID data format.	RW	00h
32h	Pwr State	Register containing the current programmed power	RW	00h

		state.		

33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.
		00h=no margin
		01h=+1 VID step
		02h=+2 VID steps
		FFh=-1 VID step
		FEh=-2 VID steps.
			RW	00h

34h	MultiVR Config			

BOOT VOLTAGE PROGRAMMING

The NCP6151/NCP6151A has a Vboot voltage register that can be externally programmed for each output. The VBOOTA also provides a feature that allows the "+1" single phase output to be disabled and effectively removed from the SVID bus. If the single phase output is disabled it alters the SVID address setting table to allow the multi-phase rail to show up at an even or odd address. See the Boot Voltage Table below.

Boot Voltage Table

Boot Voltage (V)	Resistor Value (Ohms)
0	10k
0.85	25k
0.9	45k
0.95	70k
1.0	95k
1.1	125k
1.5	165k
VCC	Shutdown (VbootA only)

ADDRESSING THE NCP6151/NCP6151A

The NCP6151/NCP6151A supports 7 possible dual SVID device addresses and 8 possible single device addresses. Pin 32 (PWM1/ADDR) is used to set the SVID address. On power up a 10uA current is sourced from this pin through a resistor connected to this pin and the resulting voltage is measured. The two tables below provide the resistor values for each corresponding SVID address. For dual addressing follow the Dual SVID Address Table. The address value is latched at startup. If VBOOTA is pulled to VCC the aux rail will be removed from the SVID bus, the address will then follow the Single Address SVID table below.

Dual SVID Address Table

Resistor Value	Main Rail SVID Address	Aux Rail SVID Address
10k	0000	0001
25k	0010	0011
45k	0100	0101
70k	0110	0111

95k	1000	1001
125k	1010	1011
165k	1100	1101

Single SVID Address Table

Resistor Value	Main Rail SVID Address (VBOOTA tied to VCC)
10k	0000
22k	0001
36k	0010
51k	0011
68k	0100
91k	0101
120k	0110
160k	0111
220k	1000

Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3V - V_{DAC}) + (V_{DROOP} - V_{CSREF})$$

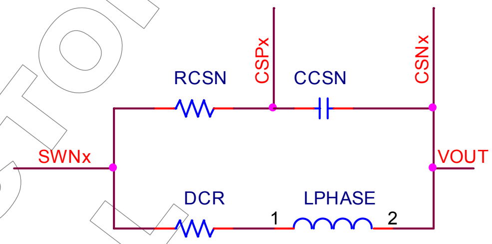
This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type 3 compensation circuit is normally used to compensate the system.

Differential Current Feedback Amplifiers

Each phase has a low offset differential amplifier to sense that phase current for current balance and per phase OCP protection during soft-start. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN not exceed 10kOhm to avoid offset issues with leakage current. It is also recommended that the voltage sense element be no less than 0.5mOhm for accurate current balance. Fine tuning of this time constant is generally not required.

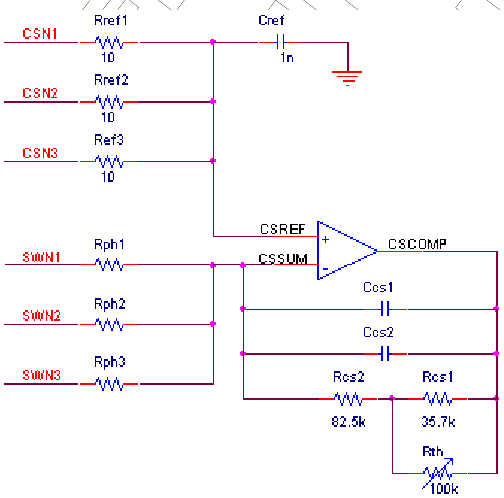


$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} * DCR}$$

The individual phase current is summed into to the PWM comparator feedback in this way current is balanced is via a current mode control approach.

Total Current Sense Amplifier

The NCP6151/NCP6151A uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.



The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1 * Rth}{Rcs1 + Rth}}{Rph} * (Iout_{Total} * DCR)$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100mV at ICCMAX then it is recommend to increase the gain of the CSCOMP amp and add a resister divider to the Droop pin filter. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 100k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25C}{2*PI*L_{Phase}}$$

$$F_P = \frac{1}{2*PI*\left(Rcs2+\frac{Rcs1*Rth@25C}{Rcs1+Rth@25C}\right)*\left(Ccs1+Ccs2\right)}$$

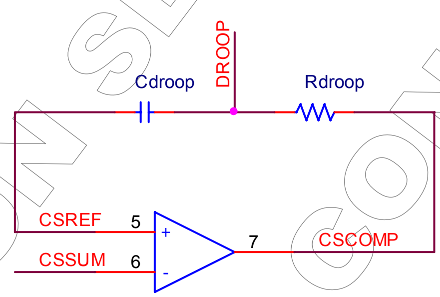
Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10uA for 50us. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15uA. Set the value of the current limit resistor based on the CSCOMP-CSREF voltage as shown below.

$$R_{LIMIT} = \frac{\frac{Rcs2+\frac{Rcs1*Rth}{Rcs1+Rth}}{Rph}*(Iout_{LIMIT}*DCR)}{10u} \quad \text{or} \quad R_{LIMIT} = \frac{V_{CSCOMP-CSREF\ @\ ILIMIT}}{10u}$$

Programming DROOP and DAC Feed-Forward Filter

The signals DROOP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage. The total current feedback should be filtered before it is applied to the DROOP pin. This filter impedance provides DAC feed-forward during dynamic VID changes. Programming this filter can be made simpler if CSCOMP-CSREF is equal to the droop voltage. Rdroop sets the gain of the DAC feed-forward and Cdroop provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.

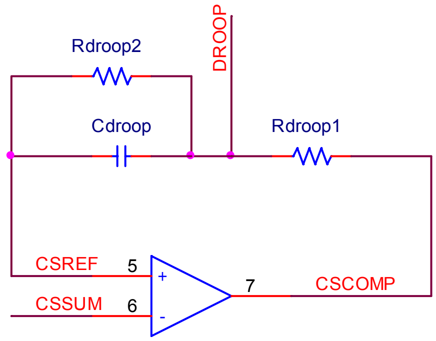


$$Rdroop = Cout * Rout * 453.6\times10^{6}$$

$$Cdroop = \frac{Rout*Cout}{Rdroop}$$

If the Droop at maximum load is less than 100mV at ICCMAX we recommend altering this filter into a voltage divider such that a larger signal can be provided to the ILIMIT resistor by increasing the CSCOMP amp gain for better current monitor accuracy. The DROOP pin divider gain should be set to provide a voltage from DROOP to

CSREF equal to the amount of voltage droop desired in the output. A current is applied to the DROOP pin during dynamic VID. In this case Rdroop1 in parallel with Rdroop2 should be equal to Rdroop



Programming IOUT

The IOUT pin sources a current equal to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2V signal on IOUT. A pull-up resistor from 5V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0V * R_{LIMIT}}{10 * \dfrac{Rcs2 + \dfrac{Rcs1 * Rth}{Rcs1 + Rth}}{Rph} * (Iout_{ICC\_MAX} * DCR)}$$

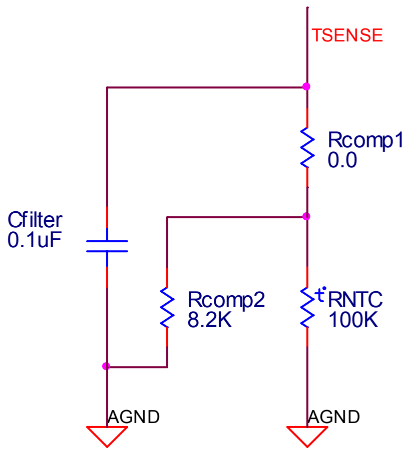
Programming ICC_MAX and ICC_MAXA

The SVID interface provides the platform ICC_MAX value at register 21h for both the multiphase and the single phase rail. A resistor to ground on the IMAX and IMAXA pins program these registers at the time the part in enabled. 10uA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1A per LSB and is set by the equation below. The resistor value should be no less than 10k.

$$ICC\_MAX_{21h} = \frac{R * 10uA * 256A}{2V}$$

Programming TSENSE and TSENSEA

Two temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE and TSENSEA pins to generate a voltage on the temperature sense network. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100k NTC similar to the VISHAY ERT-J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.



Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 100KHz/phase to 1MHz/phase. The ROSC pin provides approximately 2V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the ROSC resistor.

$$\frac{6.98kOhm \times 350kHz}{Fs} = Rosc$$

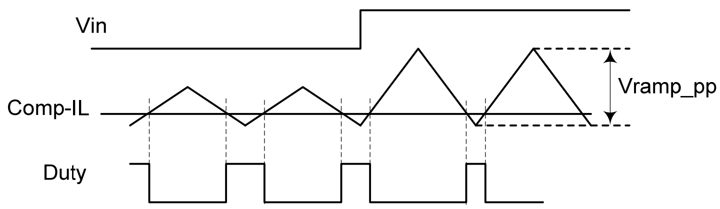
The oscillator generates triangle ramps that are 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other and the signal phase rail is set half way between phases 1 and 2 of the multi phase rail for minimum input ripple current.

Programming the Ramp Feed-Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed-forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

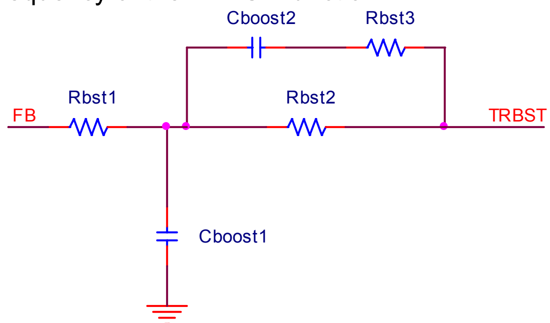
The PWM ramp time is changed according to the following,

$$V_{RAMPpk=pk_{PP}} = 0.1 * V_{VRMP}$$



Programming TRBST

The TRBST pin provides a signal to offset the output after load release overshoot. This network should be fine tuned during the board tuning process and is only necessary in systems with significant load release overshoot. The TRBST network allows maximum boost for low frequency load release events to minimize load release undershoot. The network time constants are set up to provide a TRBST roll of at higher frequencies where it is not needed. Cboost1*Rbst1 controls the time constant of the load release boost. This should be set to counter the under shoot after load release. Rbst1+ Rbst2 controls the maximum amount of boost during rapid step loading. Rbst2 is generally much larger then Rbst1. The Cboost2*Rbst2 time constant controls the roll off frequency of the TRBST function.



PWM Comparators

During steady state operation, the duty cycle is centered on the valley of the triangle ramp waveform and both edges of the PWM signal are modulated. During a transient event the duty will increase rapidly and proportionally turning on all phases as the error amp signal increases with respect to the ramps to provide a highly linear and proportional response to the step load.

PHASE DETECTION SEQUENCE

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the PWM outputs. Normally, NCP6151/NCP6151A operates as a 4-phase VCORE+1-phase VAUX PWM controller. For NCP6151/NCP6151A, Connecting PWM4 pin to VCC programs 3-phase operation.

Prior to soft start, while ENABLE is high, NCP6151/NCP6151A PWM4 pin sinks approximately 100 µA. An internal comparator checks the voltage of PWM4 pin and compares it to a threshold of hold of 2.5V. If the pin is tied to VCC, its voltage is above the threshold and the controller is configured to three phase operation otherwise the part operates in four phase mode.

The Aux rail can be disabled by pulling the VBOOTA signal to VCC. This changes the SVID address scheme to allow the multiphase to be programmed to any SVID Address odd or even. See the register resistor programming table.

Phase Count Table

Number of phases	Resistor Programming
4+1(**NCP6151/NCP6151A)**	PWM4 connected, VbootA programmed
3+1(**NCP6151)**	PWM4 tied to VCC, VbootA programmed
4+0(**NCP6151/NCP6151A)**	PWM4 connected, VbootA tied to VCC
3+0(**NCP6151)**	PWM4 tied to VCC, VbootA tied to VCC

3+1 Unused Pin Connection Table

Unused Pin	Connect to	Unused Pin	Connect to
PWM4	VCC		
CSN4	GND or VCC	CSN4	VCC
CSP4	Same as CSN4	CSP4	VCC(optional)

4+0 Unused Pin Connection Table

Unused Pin	Connect to
VBOOTA	VCC
VSPA	GND
VSNA	GND
DIFFOUTA	float
FBA	COMPA
COMPA	FBA
TRBSTA	float
CSPA	GND
CSNA	GND
CSCOMPA	CSSUMA
CSSUMA	CSCOMPA
DROOPA	GND or CSCOMPA
ILIMA	float
IMONA	GND
TSENSEA	GND
PWMA	float

3+0 Unused Pin Connection Table

Unused Pin	Connect to
PWM4	VCC
CSN4	GND or VCC
CSP4	Same as

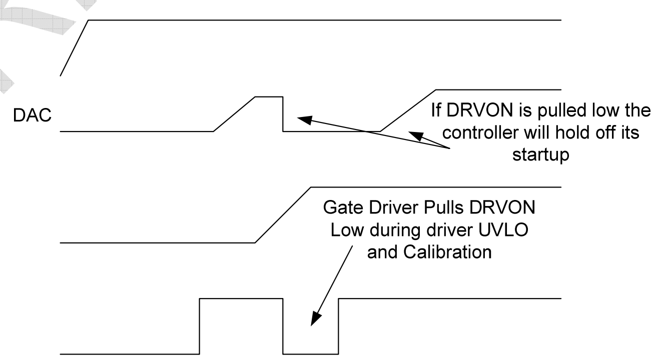
	CSN4
VBOOTA	VCC
VSPA	GND
VSNA	GND
DIFFOUTA	float
FBA	COMPA
COMPA	FBA
TRBSTA	float
CSPA	GND
CSNA	GND
CSCOMPA	CSSUMA
CSSUMA	CSCOMPA
DROOPA	GND or CSCOMPA
ILIMA	float
IMONA	GND
TSENSEA	GND
PWMA	float

Protection Features

Input Under Voltage Protection

NCP6151/NCP6151Amonitors the 5V VCC supply and the VRMP pin for under voltage protection. The gate driver monitors both the gate driver VCC and the BST voltage (12V drivers only). When the voltage on the gate driver is insufficient it will pull DRVON low and notify the controller the power is not ready. The gate driver will hold DRVON low for a minimum period of time to allow the controller to restart its startup sequence. In this case the PWM is set back to the MID state and soft start would begin again. See the figure below.

Gate Driver UVLO Restart

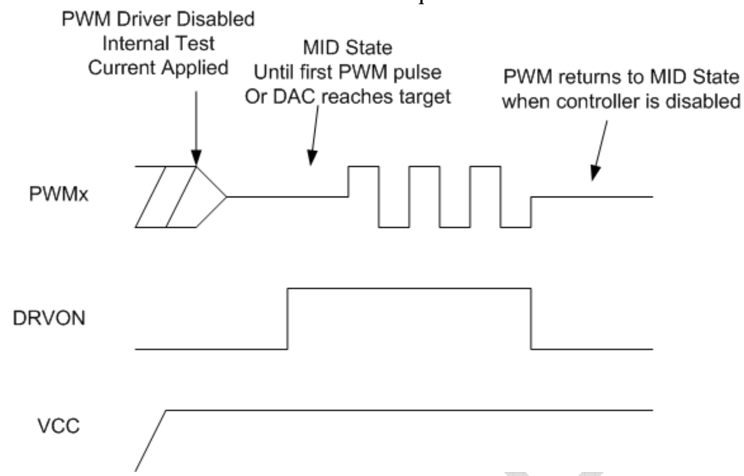


Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined slew rate in the spec table. The PWM signals will start out open with a test current to collect data on phase count and for setting internal registers. After the configuration data is collected the controller enables and sets the PWM signal to the 2.0V MID state to indicate that the drivers should be in diode mode.

DRVON will then be asserted and the COMP pin released to begin soft-start. The DAC will ramp from Zero to the target DAC codes and the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced preventing the discharge of a pre-charged output.

Soft-Start Sequence



Over Current Latch- Off Protection

The NCP6151/NCP6151 Aprovides two different types of current limit protection. During normal operation a programmable total current limit is provided that scales with the phase count during power saving operation. This limit is propramsmed with a resistor between the CSCOMP and ILIM pins. A second fixed per-phase current limit is provided for safe-start up monitoring during soft-start. The level of total current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current of 10uA and 15uA. If the current into the ILIM pin exceeds the 10A level an internal latch-off counter starts. The controller shuts down if the fault is not removed after 50us. If the current into the pin exceeds 15uA the controller will shut down immediately. To recover from an OCP fault the EN pin must be cycled low.

During startup the per phase current limit is active to protect the individual output stages. This limit monitors the voltage drop across the DCR through the CSPx and CSNx pins. The minimum threshold is.

The over-current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equation:

$$R_{ILIM} = \frac{V_{CSCOMP} - V_{CSREF}}{10uA}$$

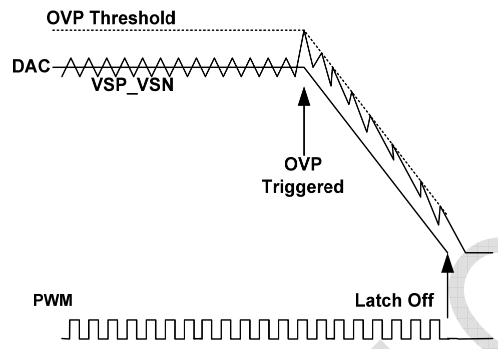
Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300mV below the DAC-DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low.

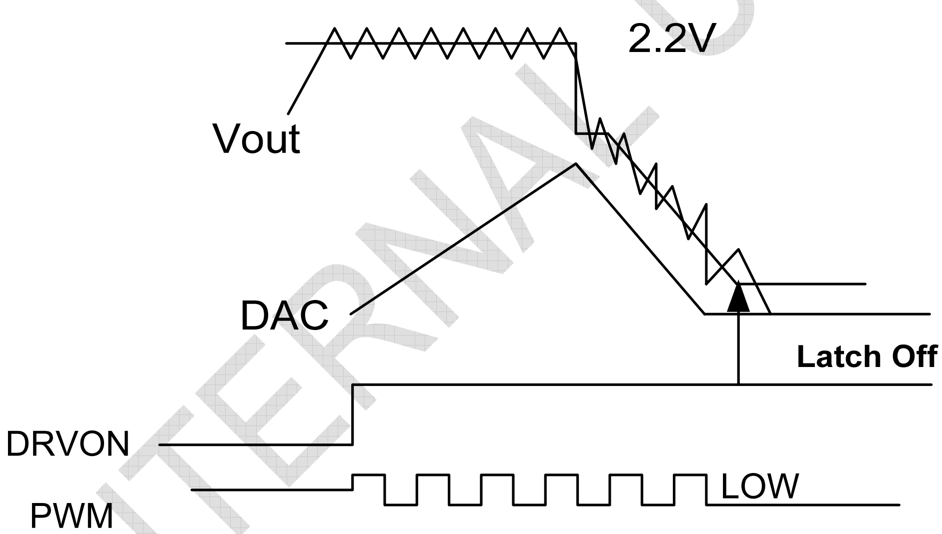
Over Voltage Protection

During normal operation the output voltage is monitored at the differential inputs VSP and VSN. If the output voltage exceeds the DAC voltage by approximately 175 mV, PWMs will be forced low until the voltage drops below the OVP threshold after the first OVP trip the DAC will ramp down to zero to avoid a negative output voltage spike during shutdown. When the DAC gets to zero the PWMs will be forced low and the DRVON will remain high. To reset the part the Enable pin must be cycled low. During soft-start, the OVP threshold is set to 2.2V. This allows the controller to start up without false triggering the OVP. Prior to soft-start the gate drivers will provide OVP protection directly at the switching nodes.

OVP Threshold Behavior



Start up OVP Threshold Behavior



Layout Notes

The NCP6151/NCP6151A has differential voltage and current monitoring. This improves signal integrity and reduces noise issues related to layout for easy design use. To insure proper function there are some general rules to follow. Always place the inductor current sense RC filters as close to the CSN and CSP pins on the controller as possible. Place the VCC decoupling caps as close as possible to the controller VCC pin. The high frequency filter cap on CSREF and the 10 ohm CSREF resistors should be placed close to the controller. The small high feed back cap from COMP to FB should be as close to the controller as possible. Please minimize the capacitance to ground of the FB traces by keeping them short. The filter cap from CSCOMP to CSREF should also be close to the controller.

QFN52 6x6 0.65P PACKAGE DIMENSIONS

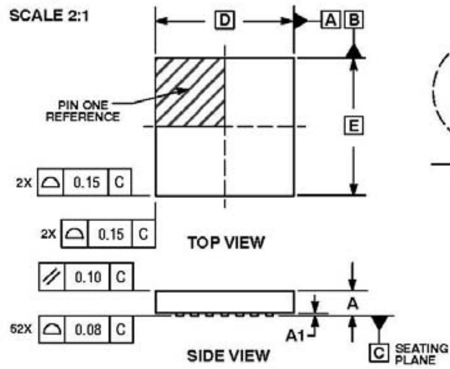
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

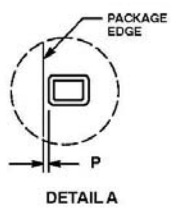
ON Semiconductor®

QFN52 6x6, 0.65P
CASE 485AV−01
ISSUE A

DATE 29 OCT 2008

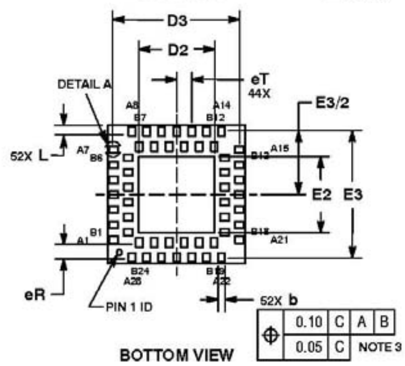
SCALE 2:1



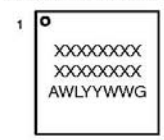


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX
A	0.80	0.90	1.00
A1	0.00	0.05	0.10
b	0.25	0.30	0.35
D		6.00 BSC	
D2	3.20	3.30	3.40
D3		5.50 BSC	
E		6.00 BSC	
E2	3.20	3.30	3.40
E3		5.50 BSC	
eT		0.65 BSC	
eR		0.65 BSC	
L	0.35	0.40	0.45
P		0.05 REF	



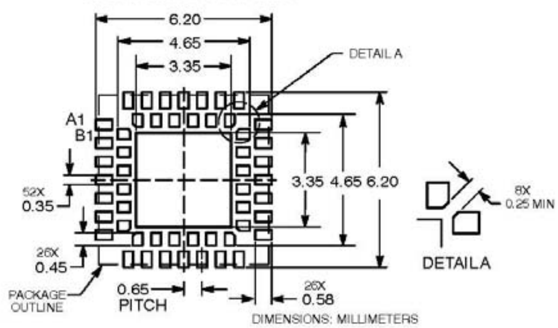
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERING FOOTPRINT



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NEW STANDARD:		
DESCRIPTION:	**QFN52 6x6, 0.65P**	**PAGE 1 OF 2**